1-wire communication

1 1-wire bus

An 1-wire bus is based on a serial protocol using only a single data line plus ground reference for communication. A 1-wire master initiates and controls the communication with one or more 1-wire slave devices on the 1-wire bus.

Each 1-wire slave device features a unique, unalterable, factory-programmed, 64-bit ID (identification number), which serves as device address on the 1-wire bus. The 8-bit family code, a subset of the 64-bit ID, identifies the device type and functionality. Typically, 1-wire slave devices operate over the voltage range of 2.8 V (min) to 5.25 V (max) and most 1-Wire devices have no pin for power supply; they take their energy from the 1-wire bus (known as parasitic supply).

2 1-wire communication protocol

Several signal types are defined by this protocol: reset pulse, presence pulse, write 0, write 1, read 0, and read 1. The bus master initiates all these signals, with the exception of the presence pulse.

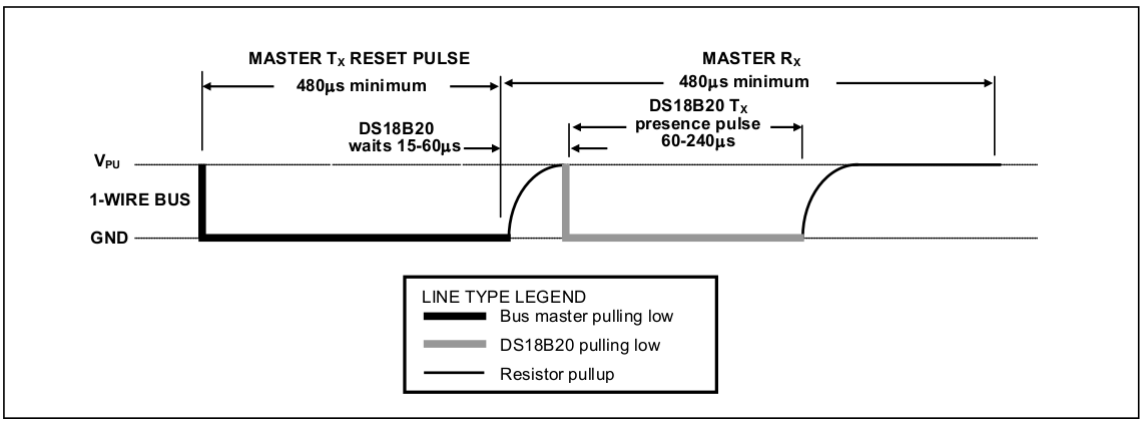
2.1 Initialization procedure: Reset and presence pulses

All communication with any 1-wire slave device begins with an initialization sequence that consists of a reset pulse from the master followed by a presence pulse from any 1-wire slave device.

When a 1-wire slave device sends the presence pulse in response to the reset, it is indicating to the master that it is on the bus and ready to operate.

During the initialization sequence the bus master transmits the reset pulse by pulling the 1-wire bus low for a minimum of 480µs.

The bus master then releases the bus and goes into receive mode. When the bus is released, the 5 kΩ pullup resistor pulls the 1-wire bus high. When a 1-wire slave device detects this rising edge, it waits 15µs to 60µs and then transmits a presence pulse by pulling the 1-wire bus low for 60µs to 240µs.



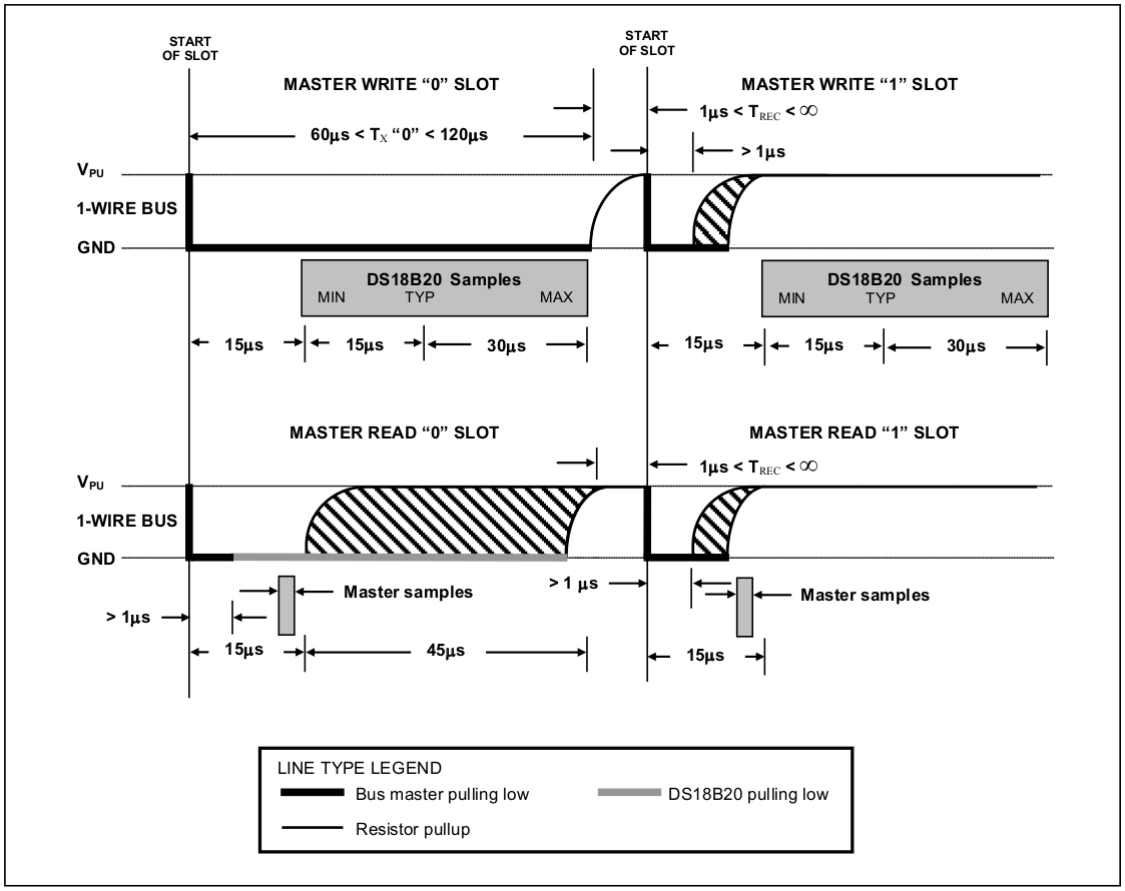
The bus master writes data to a 1-wire slave device during write time slots and reads data from a 1-wire slave device during read time slots. One bit of data is transmitted over the 1-wire bus per time slot.

2.2 Write time slots

There are two types of write time slots: “Write 1” time slots and “Write 0” time slots. The bus master uses a Write 1 time slot to write a logic 1 to a 1-wire slave device and a Write 0 time slot to write a logic 0 to the 1-wire slave device. All write time slots must be a minimum of 60 µs in duration with a minimum of a 1 µs recovery time between individual write slots. Both types of write time slots are initiated by the master pulling the 1-wire bus low.

To generate a Write 1 time slot, after pulling the 1-wire bus low, the bus master must release the 1-Wire bus within 15 µs. When the bus is released, the 5 kΩ pullup resistor will pull the bus high. To generate a Write 0 time slot, after pulling the 1-Wire bus low, the bus master must continue to hold the bus low for the duration of the time slot (at least 60 µs).

A 1-wire slave device samples the 1-wire bus during a window that lasts from 15 µs to 60 µs after the master initiates the write time slot. If the bus is high during the sampling window, a 1 is written to the 1-wire slave device. If the line is low, a 0 is written to the 1-wire slave device.

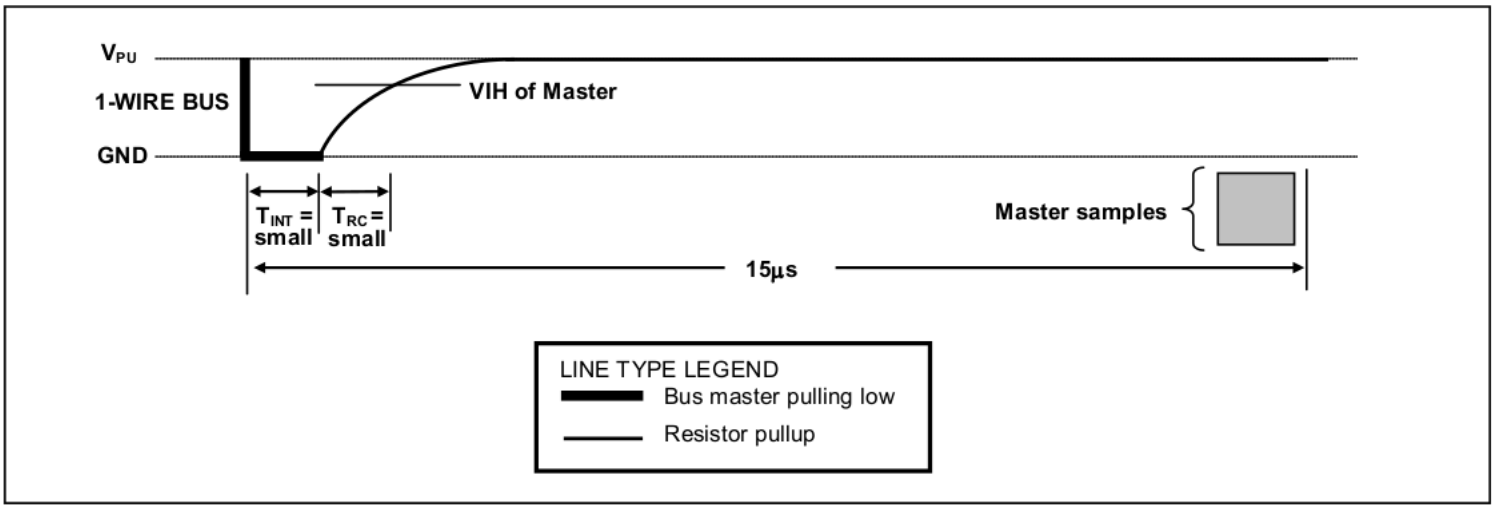


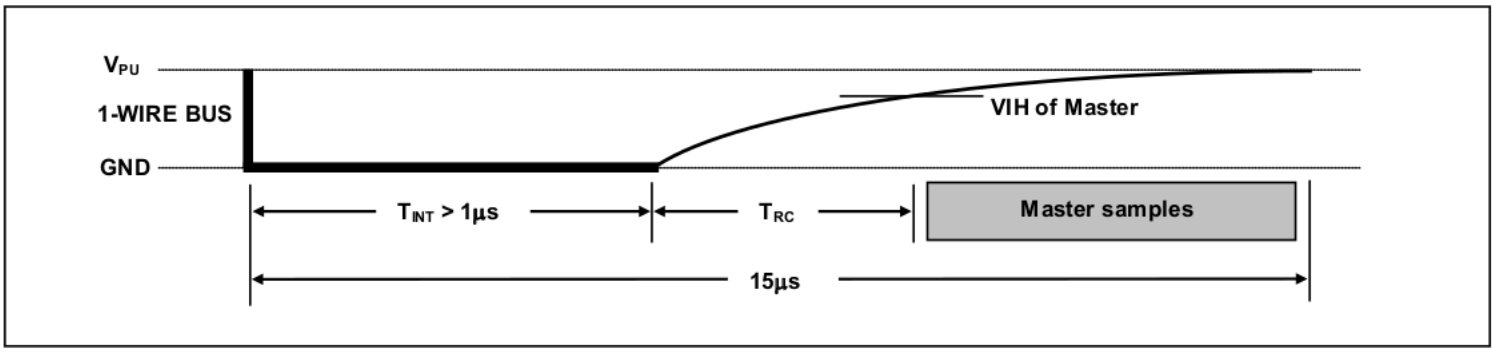
2.3 Read time slots

A 1-wire slave device can only transmit data to the master when the master issues read time slots. Therefore, the master must generate read time slots immediately after issuing a commands, so that the slave device can provide the requested data.

All read time slots must be a minimum of 60 µs in duration with a minimum of a 1 µs recovery time between slots. A read time slot is initiated by the master device pulling the 1-wire bus low for a minimum of 1 µs and then releasing the bus.

After the master initiates the read time slot, the 1-wire slave device will begin transmitting a 1 or 0 on bus. The device transmits a 1 by leaving the bus high and transmits a 0 by pulling the bus low. When transmitting a 0, the device will release the bus by the end of the time slot, and the bus will be pulled back to its high idle state by the pullup resistor. Output data from the device is valid for 15 µs after the falling edge that initiated the read time slot. Therefore, the master must release the bus and then sample the bus state within 15 µs from the start of the slot.





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